

ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device includes an address buffer which receives an address signal that indicates an address of a memory cell array, a latch  
5 circuit which latches the data, and an address transition detection circuit which detects transition of the address. During the access operation of the memory cell array, an address at the operation start time is latched by the latch circuit. After the end of  
10 the operation of the memory cell array, an address that is currently input to the address buffer is latched by the latch circuit. If the received address signal is data different from the latch data, a control signal that controls the cycle operation of the memory cell  
15 array for a predetermined period is generated on the basis of the detection result from the address transition detection circuit.